IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of	:	
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First Named Inventor: Gilbert Christopher Sih	:	**Confirmation No.** 3901
	:	
U.S. Patent Application No. 10/807,648	:	**Group Art Unit:** 2188
	:	
Filed: March 24, 2004	:	**Examiner:** Song, Jasmine

For: CACHED MEMORY SYSTEM AND CACHE CONTROLLER FOR EMBEDDED DIGITAL SIGNAL PROCESSOR

BRIEF ON APPEAL UNDER 37 C.F.R. § 41.37

REVISED SUMMARY OF CLAIMED SUBJECT MATTER

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Further to the Notice of Non-Compliant Appeal filed October 27, 2008, in connection with the above-identified application on appeal, the Appellant respectfully submits this revised Summary of Claimed Subject Matter section, which addresses independent claims 1, 12 and 14. Please charge any fees or credit any overpayments that may be due with this Brief to Deposit Account No. 17-0026.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Claim 1 is directed to an integrated circuit (IC) (e.g., see 300, 400, 920 of Figures 3, 4 and 9, respectively) including a processor core (e.g., see 330, 430 of Figures 3 and 4, respectively) operable to perform data processing for the integrated circuit, a cache memory (e.g., see 340, 440a/b/x of Figures 3 and 4, respectively) operable to store data for the processor core and an on-chip memory (e.g., see 350, 450 of Figures 3 and 4, respectively) operable to store data for the cache memory, wherein the cache memory is filled with data from the on-chip memory for cache misses, and wherein the on-chip memory is selectably filled with data from an external memory (e.g., see 360, 460 of Figures 3 and 4, respectively) independent of cache accesses of the cache memory under user control (e.g., see [0037], "[o]ne advantage of cached memory system 300 is that the user/programmer can arrange to have the instructions and data required by processor core 330 to be present in on-chip memory 350 well in advance of when they are actually needed by the processor core. A conventional level 2 cache controller would only fetch instructions and data if and when they are needed by the processor core …).

Claim 12 is directed to a wireless apparatus (900) including an integrated circuit (e.g., see 300, 400, 920 of Figures 3, 4 and 9, respectively) including a processor core (e.g., see 330, 430 of Figures 3 and 4, respectively) operable to perform data processing, a cache memory (e.g., see 340, 440a/b/x of Figures 3 and 4, respectively) operable to store data for the processor core, and an on-chip memory (e.g., see 350, 450 of Figures 3 and 4, respectively) operable to store data for the cache memory. The apparatus of claim 12 further includes an external memory (e.g., see 360, 460 of Figures 3 and 4, respectively) operable to store data for the on-chip memory, wherein the cache memory is filled with data from the on-chip memory for cache misses, and wherein the on-chip memory is selectably filled with data from the external

memory independent of cache accesses of the cache memory under user control (e.g., see [0037], "[o]ne advantage of cached memory system 300 is that the user/programmer can arrange to have the instructions and data required by processor core 330 to be present in on-chip memory 350 well in advance of when they are actually needed by the processor core. A conventional level 2 cache controller would only fetch instructions and data if and when they are needed by the processor core …).

Claim 14 is directed to an integrated circuit (920), including a first processor (922) operable to perform general-purpose processing for the integrated circuit, a second processor (924) operable to perform data processing for the integrated circuit and including a processor core (e.g., see 330, 430 of Figures 3 and 4, respectively)operable to perform the data processing, and a first cache memory (e.g., see 340, 440a/b/x of Figures 3 and 4, respectively) operable to store data for the processor core, an on-chip memory (e.g., see 350, 450 of Figures 3 and 4, respectively) operable to store data for the first cache memory, wherein the first cache memory is filled with data from the on-chip memory for cache misses, and wherein the on-chip memory is selectably filled with data from an external memory (e.g., see 360, 460 of Figures 3 and 4, respectively) independent of cache accesses of the first cache memory under user control and a first memory bus (e.g., see 928 of Figure 9) coupling the first and second processors to the external memory (e.g., see [0037], "[o]ne advantage of cached memory system 300 is that the user/programmer can arrange to have the instructions and data required by processor core 330 to be present in on-chip memory 350 well in advance of when they are actually needed by the processor core. A conventional level 2 cache controller would only fetch instructions and data if and when they are needed by the processor core …).

CONCLUSION

The Appellant respectfully submits that claims 1-5, 7-8, 10-18 and 35-54 are patentable over the applied art and that all of the rejections and objections of record should be reversed.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 17-0026 for any additional fees required under 37 C.F.R. § 1.16 or 1.17, particularly extension of time fees.

Respectfully submitted,

Dated: November 24, 2008

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